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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,653	11/09/2001	Fernando Gonzalez	98095DIV4	8023

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KIRKPATRICK & LOCKHART LLP
535 SMITHFIELD STREET
PITTSBURGH, PA 15222

EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,653	GONZALEZ ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17,19,98-103,125,126 and 128* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17,19,98-103,125,126 and 128* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The declaration filed on 1/13/03 under 37 CFR 1.131 is sufficient to overcome the Wu and Ono references.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 17, 19, 98-101, 103, 125, 126 and 128 are rejected under 35 U.S.C. 102(b) as being anticipated by Moravvej-Farshi et al. ("Novel Self-Aligned Polysilicon-Gate MOSFETs with Polysilicon Source and Drain," Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-62).

Moravvej-Farshi et al. disclose in figure 6 a raised drain structure (n+ poly), a raised source structure (n+ poly), a gate (n+ poly) located between the source and drain, a first capping layer (silicon dioxide on left half of figure) in communication with at least a portion of the gate and source, a first portion of a gate oxide region in communication with at least a portion of the gate and source, a first implant junction area (dashed line beneath source) located in the substrate assembly extending partially beneath the gate and the source, a second capping layer (silicon dioxide on right half of figure) in communication with at least a portion of the gate and drain, a second portion

of a gate oxide region in communication with at least a portion of the gate and drain, and a second implant junction area (dashed line beneath drain) located in the substrate assembly extending partially beneath the gate and the drain.

With regard to claim 19, the first and second junctions include doped areas.

With regard to claim 98, the raised source is doped polysilicon.

With regard to claim 99, the raised drain is doped polysilicon.

With regard to claim 100, the gate is doped polysilicon.

With regard to claim 101, the source includes a plug.

With regard to claim 103, the gate includes a gate terminal as the entire gate structure is considered the gate terminal.

With regard to claim 125, Moravvej-Farshi et al. disclose in figure 6 a raised drain structure (n+ poly), a raised source structure (n+ poly), a gate (n+ poly) located between the source and drain, a first capping layer (silicon dioxide on left half of figure) in communication with at least a portion of the gate and source, a first portion of a gate oxide region in communication with at least a portion of the gate and source, a first implant junction area (dashed line beneath source) located in the substrate assembly extending partially beneath the gate and the source wherein the first junction are includes doped silicon, a second capping layer (silicon dioxide on right half of figure) in communication with at least a portion of the gate and drain, a second portion of a gate oxide region in communication with at least a portion of the gate and drain, and a second implant junction area (dashed line beneath drain) located in the substrate

assembly extending partially beneath the gate and the drain wherein the second junction area includes doped silicon.

With regard to claim 126, the doped silicon includes phosphorous.

With regard to claim 128, Moravvej-Farshi et al. disclose in figure 6 a raised drain structure (n+ poly), a raised source structure (n+ poly), a gate (n+ poly) located between the source and drain, a first capping layer (silicon dioxide on left half of figure) in communication with at least a portion of the gate and source, a first portion of a gate oxide region in communication with at least a portion of the gate and source, a first implant junction area (dashed line beneath source) located in the substrate assembly extending partially beneath the gate and the source wherein the first junction includes a pocket implant junction, a second capping layer (silicon dioxide on right half of figure) in communication with at least a portion of the gate and drain, a second portion of a gate oxide region in communication with at least a portion of the gate and drain, and a second implant junction area (dashed line beneath drain) located in the substrate assembly extending partially beneath the gate and the drain wherein the second junction area includes a pocket implant junction.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 102 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moravvej-Farshi et al. ("Novel Self-Aligned Polysilicon-Gate MOSFETs with Polysilicon Source and Drain," Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-62).

Moravvej-Farshi et al. teach a plug on the source but do not teach an adhesive layer included in the plug. The plug of Moravvej-Farshi et al. is taught as comprising aluminum and the source region is silicon. Official Notice is taken that it is well known in the art to form an adhesion/barrier layer between aluminum plugs and silicon regions. TiN or WN are commonly formed on a silicon source region to prevent an aluminum plug from diffusing into the silicon and leaving voids at the contact between the silicon and the aluminum. One of ordinary skill in the art at the time of the invention would have been motivated to provide a barrier/adhesion layer to prevent the aluminum diffusion and the resultant increase in resistivity. Thus, it would have been obvious to provide the layer as claimed in claim 102.

Response to Arguments

6. Applicant's arguments filed with non-responsive amendments B and C are moot in light of the presently presented claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR
July 25, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800